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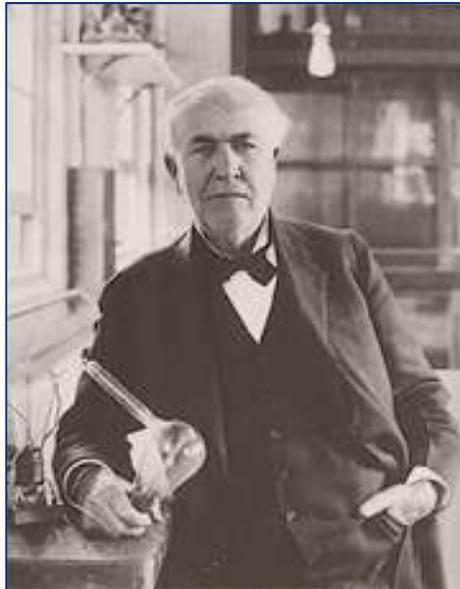
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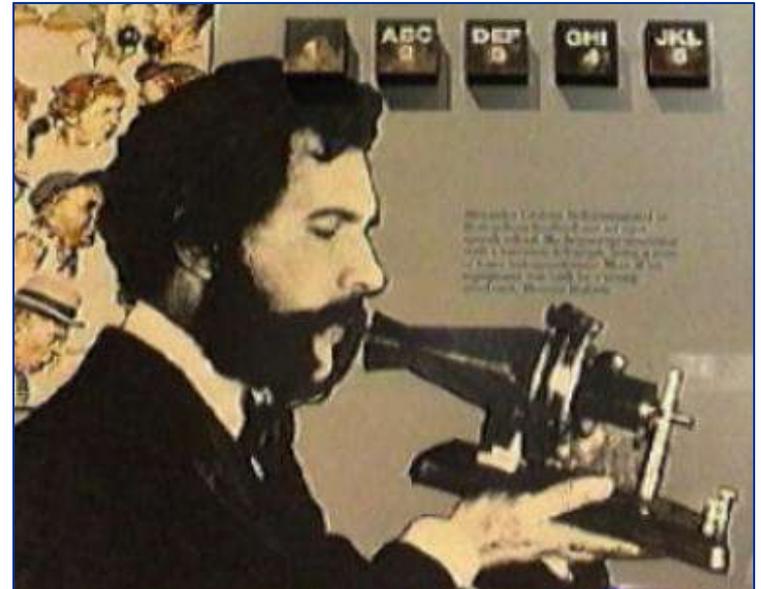
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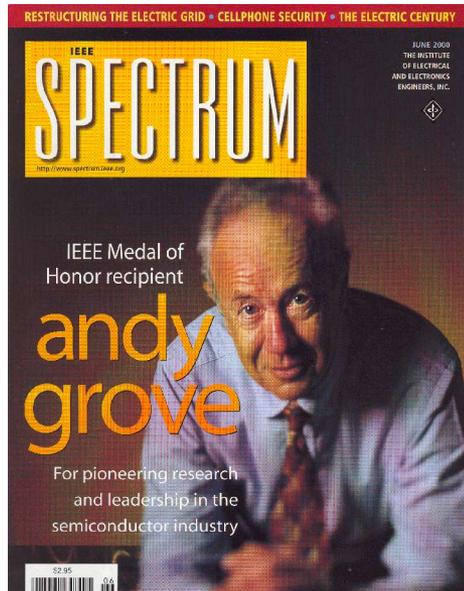
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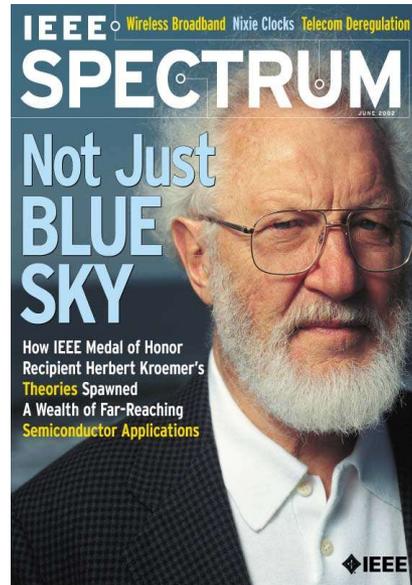


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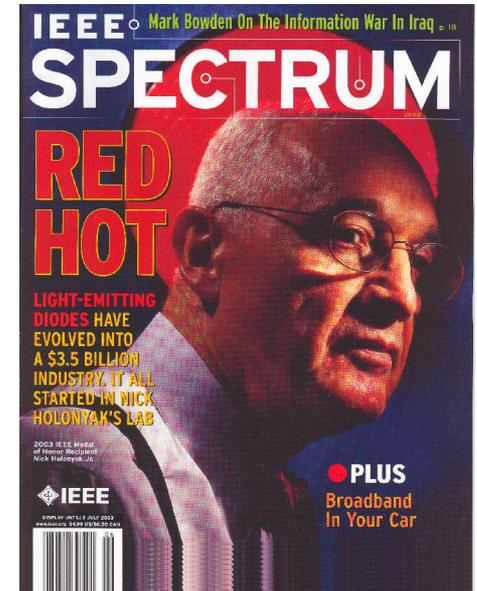
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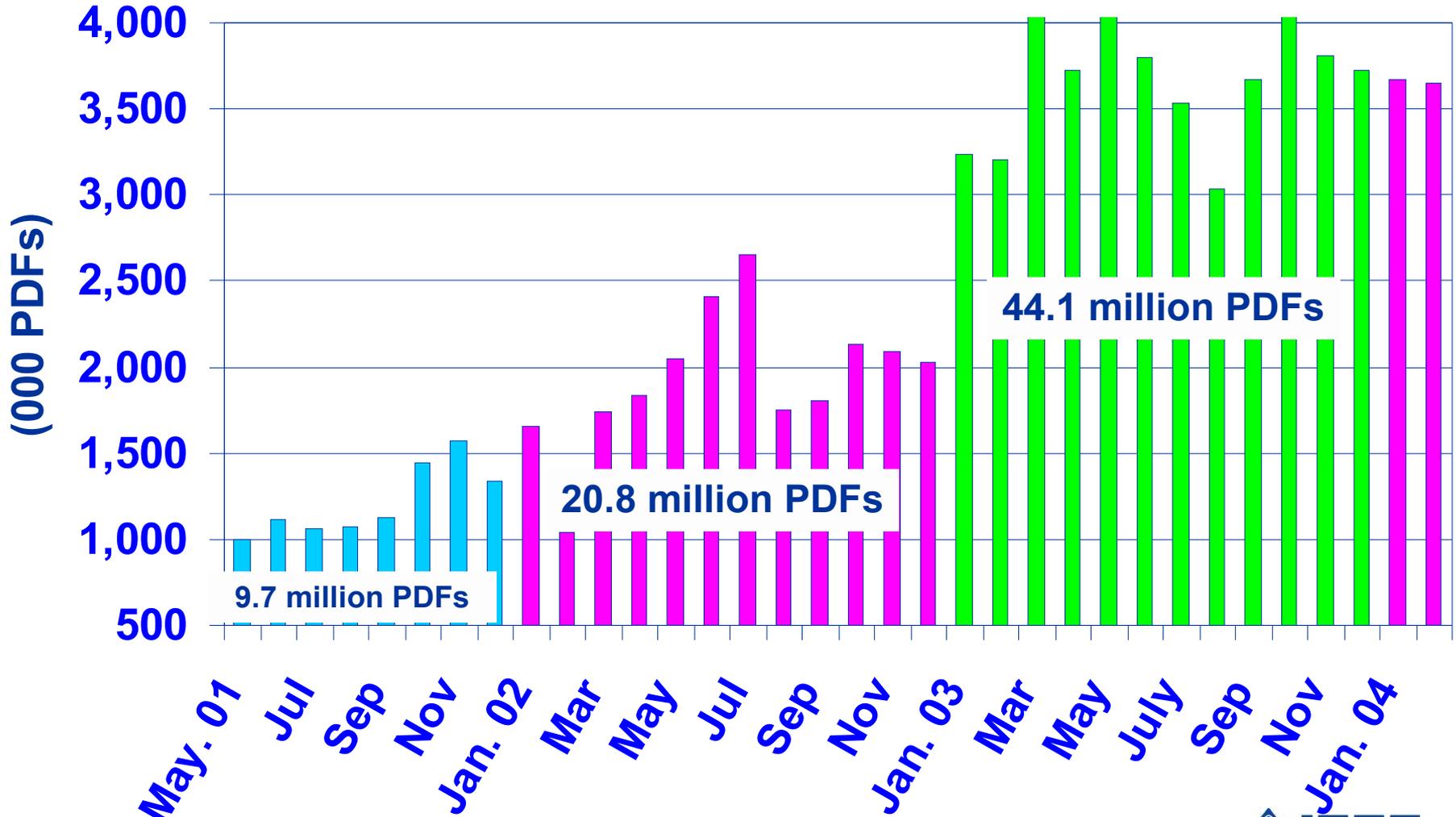
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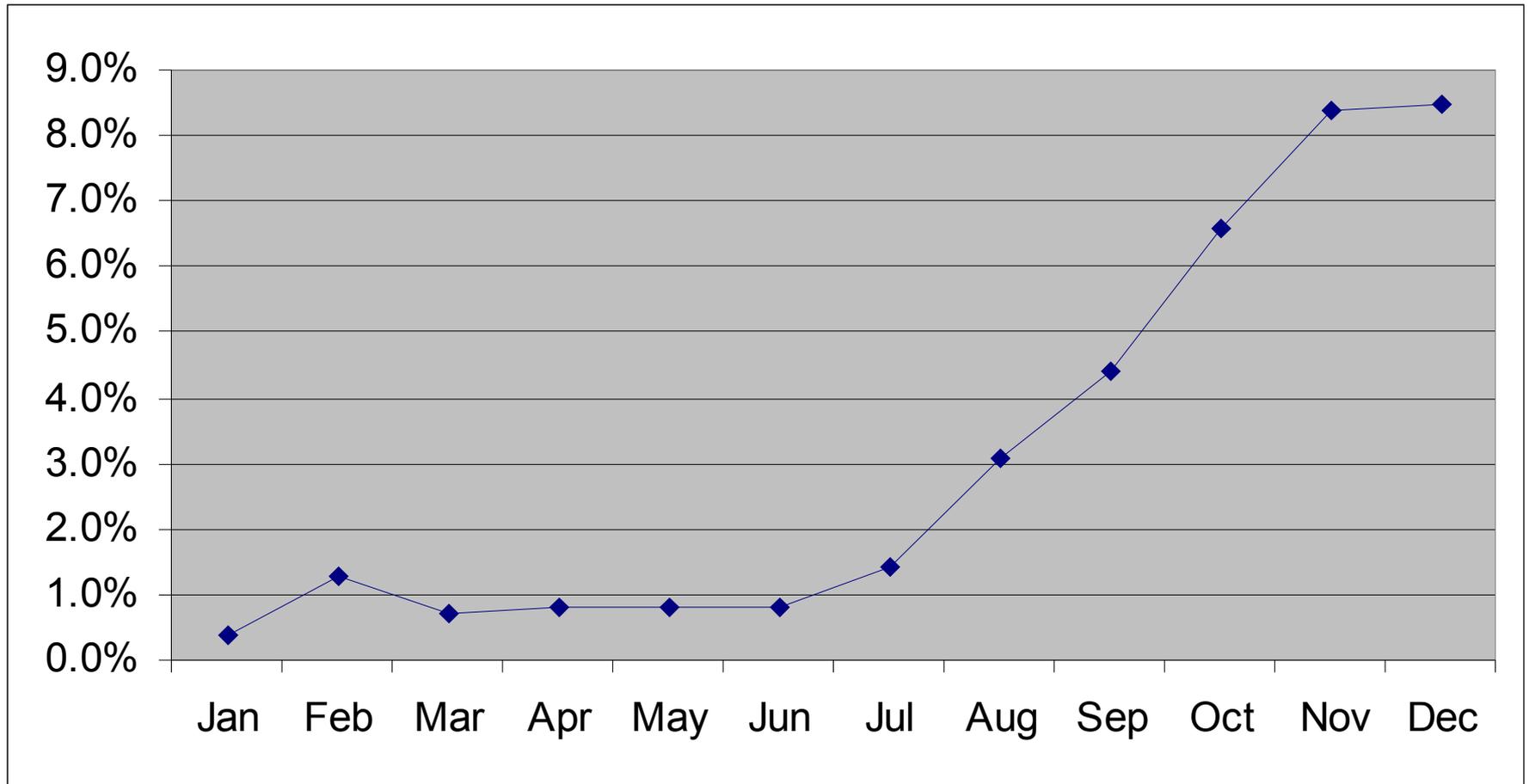
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Sangrok Lee

Abstract—A 32×16 liquid-crystal-on-silicon (LCOS) backplane with novel frame buffer pixel circuit using the AMI Semiconductor's 0.5- μm double-poly triple-metal CMOS process. The three novel pixel circuits described herein increase the brightness of an XGA LCOS microdisplay by at least 26% without sacrificing image contrast ratio. The increase of brightness is attributed to maximizing overall image view time, allowing an image to be displayed at full contrast while the next image is buffered onto the backplane. The new circuits achieve this by removing charge sharing and charge induction problems shown in previously proposed frame buffer pixel circuits. Voltages on the pixel electrodes measured through rail-to-rail operational amplifiers with negative feedback vary from 0 to 4.25 V (6-V power source). All data voltage levels remain constant over a frame time with less than 1% drop, thus ensuring maximum contrast ratio. Modeling and experimental measurement on the fabricated chip show that these pixel circuits outperform all others to date based on storage time, data storage level, and potential for highest contrast ratio with maximum brightness.

Index Terms—Frame buffer pixel, liquid-crystal-on-silicon (LCOS), microdisplay.

LIQUID-crystal-on-silicon (LCOS) microdisplays utilize high birefringence and low operating voltage liquid crystal (LC) materials aligned on top of a single crystal silicon circuit to control and maintain the director distribution of the LC for high-resolution small-sized displays [3]. Single crystal silicon VLSI technology is well recognized as a competitive alternative to active matrix liquid crystal display (AMLCD) [4]. The advantages include higher electron mobility producing better electron characteristics and the use of more mature, off-the-shelf technology. Furthermore, complicated column and row driver circuits and pixel arrays can be achieved through a

Novel Frame Buffer Pixel Circuits for Liquid-Crystal-on-Silicon Microdisplays

Sangrok Lee, Member, IEEE

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Sangrok Lee, Member, IEEE, James C. Morizio, Member, IEEE, and Kristina M. Johnson, Fellow, IEEE

Abstract—A 32×16 liquid-crystal-on-silicon (LCOS) backplane with novel frame buffer pixel circuit is designed and fabricated using the AMI Semiconductor's 0.5- μm double-poly triple-metal CMOS process. The three novel pixel circuits described herein increase the brightness of an XGA LCOS microdisplay by at least 26% without sacrificing image contrast ratio. The increase of brightness is attributed to maximizing overall image view time, allowing an image to be displayed at full contrast while the next image is buffered onto the backplane. The new circuits achieve this by removing charge sharing and charge induction problems shown in previously proposed frame buffer pixel circuits. Voltages on the pixel electrodes measured through rail-to-rail operational amplifiers with negative feedback vary from 0 to 4.25 V (6-V power source). All data voltage levels remain constant over a frame time with less than 1% drop, thus ensuring maximum contrast ratio. Modeling and experimental measurement on the fabricated chip show that these pixel circuits outperform all others to date based on storage time, data storage level, and potential for highest contrast ratio with maximum brightness.

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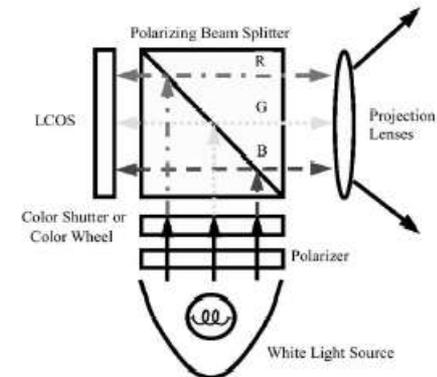


Fig. 1. Field sequential color projection display with a single microdisplay.

One of the main applications of LCOS technology is in projection display systems. The front projector is very commonly used in business and educational settings, while rear projection displays are considered promising candidates for home theater systems. The contemporary standard LCOS projection display uses three microdisplay panels, one for each primary color. The advantage of the three-panel design is that the images have maximum brightness. However, the disadvantage is the need for complicated and expensive optics to separate the colors and difficulty in alignment of red, green, and blue images, which increases manufacturing cost. These disadvantages go away with single panel architecture known as field sequential color (FSC)

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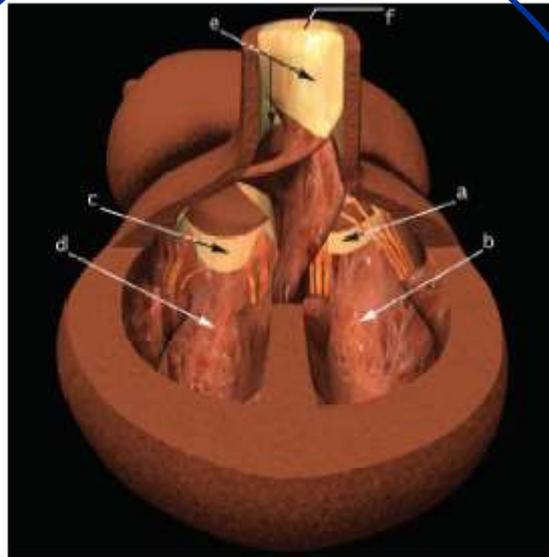
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there were only a few matte objects. Without losing realism, we chose a rendering without shadows and multiple reflections. LightWave stores the rendered images of the sequence in the Targa32 format. The image resolution is 728×576 pixels to match the picture to the European PAL video standard. We used Adobe Premiere to edit the final animation, which is available in AVI format. (You can view two examples at <http://virtual-heart-development.univ-rennes1.fr/anglais/generale.htm> by clicking on the "Animations" button.) However, this animation isn't always self-explanatory. We post-processed oral explanations and identification signs on the video to describe precisely the anatomy and its mutation and to highlight some particularities of this anatomy or some specific phenomena. The objective of the animation is to teach the normal heart development. The final animation is about 12 minutes long with more than 18,000 frames.

Results

The overall process of the model design from the medical definition of the sequence to the final modeling and validation took about three years. The figures presented here highlight some important stages of the overall cardiac morphogenesis. Chronologically, the first visible phase is fertilization (Figure 5). In this sequence,



6 The mitral (a) and tricuspid (c) valves separating, respectively, the left and right atria from the corresponding ventricle. This model of the opened heart shows the mitral valve (a) and left ventricle (b), tricuspid valve (c) and right ventricle (d), aorta (e), and pulmonary artery (f).

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2) Functions

$$f_{i,t} : \mathbb{R}^{t-1} \times \{1, 2, \dots, 2^{\lceil R_i \rceil}\} \rightarrow \mathbb{R}, \quad t = 1, 2, \dots, T$$

for the source nodes $i \in \mathcal{S}$ and $f_{j,t} : \mathbb{R}^{t-1} \rightarrow \mathbb{R}, t = 2, \dots, T$ for all the other nodes $j \notin \mathcal{S}$, such that

$$X_i(t) = f_{i,t}(Y_i(1), \dots, Y_i(t-1), \overline{W}_i), \quad t = 1, 2, \dots, T$$

$$X_j(1) = 0, \quad X_j(t) = f_{j,t}(Y_j(1), \dots, Y_j(t-1)), \quad t = 2, 3, \dots, T$$

such that the following total power constraint holds:

$$\frac{1}{T} \sum_{t=1}^T \sum_{i \in \mathcal{N}} X_i^2(t) \leq P_{\text{total}}, \quad \text{a.s.} \quad (1)$$

3) m decoding functions

$$g_\ell : \mathbb{R}^T \times \{1, 2, \dots, \lceil \overline{W}_{d_\ell} \rceil\} \rightarrow \{1, 2, \dots, 2^{\lceil R_\ell \rceil}\}$$

for the destination nodes of the m source-destination pairs $\{(s_\ell, d_\ell), \ell = 1, \dots, m\}$, where $\lceil \overline{W}_{d_\ell} \rceil$ is the number of different values \overline{W}_{d_ℓ} can take. Note that \overline{W}_{d_ℓ} may be empty.

4) The average probability of error:

$$P_e^{(T)} := \text{Prob}(\{(\hat{W}_1, \hat{W}_2, \dots, \hat{W}_m) \neq (W_1, W_2, \dots, W_m)\}) \quad (2)$$

where $\hat{W}_\ell := g_\ell(Y_{d_\ell}^T, \overline{W}_{d_\ell})$, with

$$Y_{d_\ell}^T := (Y_{d_\ell}(1), Y_{d_\ell}(2), \dots, Y_{d_\ell}(T)).$$

Definition 2.3: The network's transport capacity C_T is

$$C_T := \sup_{(R_1, \dots, R_m) \text{ feasible}} \sum_{\ell=1}^m R_\ell \cdot \rho_\ell$$

where for brevity $\rho_\ell := \rho_{s_\ell d_\ell}$ denotes the distance between s_ℓ and d_ℓ , and $R_\ell := R_{s_\ell d_\ell}$.

This is the supremum distance-weighted sum of rates that the network can deliver. The units in which it is measured is bit-

meters per second per Hz per meter. This is the supremum distance-weighted sum of rates that the network can deliver. The units in which it is measured is bit-meters per second per Hz per meter. This is the supremum distance-weighted sum of rates that the network can deliver. The units in which it is measured is bit-meters per second per Hz per meter.

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exceeds the upper bound on the transport capacity.

Third, whenever a rate vector is feasible, and is such that its distance-weighted sum of rates is close to the transport capacity, then one can rest assured that the network is being operated close to capacity. We will see that this situation actually holds.

Potential Formalisms in Electromagnetic-Field Analysis

GEORGIEVA AND TAM: POTENTIAL FORMALISMS IN EM-FIELD ANALYSIS

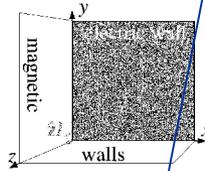


Fig. 1. Computational volume of the dipole radiating

The operator $\nabla^2 - \mathcal{T}_{\mu\epsilon}$ defaults to the well-known $\nabla^2 - \mu\epsilon\partial_{tt}$ in a loss-free medium. Notice that to the "ordinary" vector potentials as

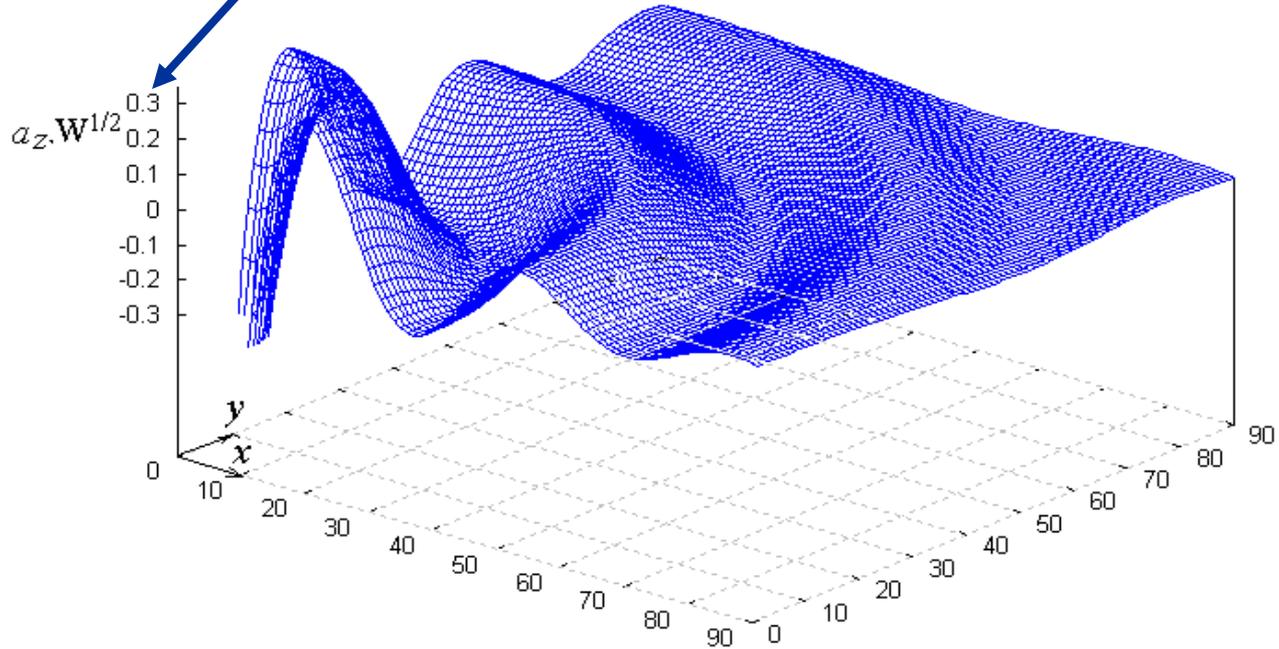
$$\begin{aligned} \mathbf{A}_\mu &= \mu^{-1} \mathbf{A} \\ \mathbf{F}_\epsilon &= \epsilon^{-1} \mathbf{F}. \end{aligned}$$

As a first example, let us consider the E-field of a very small dipole (electric current element) we set as $\mathbf{J}_e = \hat{\mathbf{z}}J_{ez}$ in the $x=0-y$ -plane. According to equation (13), a spherical $\mathbf{A}_\mu = \hat{\mathbf{z}}A_{\mu z}$ wave propagates in open space. We examine this wave when the sinusoidal function of time.

We simulate numerically this problem using a reference algorithm based on the time-domain (TDWP) approach [28], which solves the equations with specified boundary conditions and medium. The computational volume (see Fig. 1) includes only one octant of the symmetry of the problem. There is a magnetic wall at $z = 0$ and magnetic walls at $x = 0$ and $y = 0$. The three boundaries employ absorbing boundary conditions to simulate reflection-free propagation. The normalized potentials $\mathbf{a} = \sqrt{Z_0} \mathbf{A}_\mu$ and \mathbf{f} measured in $W^{1/2}$. Here, $Z_0 = \sqrt{\mu_0/\epsilon_0}$ is the impedance of vacuum.

In the z -oriented dipole example, a single normalized potential $a = \hat{\mathbf{z}}a_z$ is computed and the wave in the $x=0-y$ -plane is animated in the x - y plane. In all examples considered in this paper, the computational volume is discretized into a uniform mesh. For the example we choose a spatial step size $\Delta h = \lambda/30$, where λ is the wavelength in free space corresponding to the frequency of the excitation current ($\lambda = 1$ m). The x - and y -axes in the animation are scaled in terms of the spatial step Δh . For example, the point (30, 45) has actual coordinates $x = 30\Delta h$, $y = 45\Delta h$ with respect to the

A picture is worth dozens of equations:
This animation shows how these formulas allow an engineer to predict the actions of an electro-magnetic field (a radio wave) as it leaves an antenna



$$-\mathcal{T}_\mu \Psi = \nabla \cdot \mathbf{F}_\epsilon. \tag{20}$$

The vector operators $(\nabla \mathcal{T}_\epsilon)$ and $(\nabla \mathcal{T}_\mu)$ are the gradients of the operators defined in (14) as follows:

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BREAKER PAGE

Patents are Significant New Measures of Value

- **CHI Research, Inc. Research Consultancy based in New Jersey – examines patents as predictor of a company’s market value.**
 - **Patent portfolio is a product of R&D spending**
 - **Most valuable patents cite research papers (“science linkage”) vs. other patents**
 - **Science linkage means idea is closer to basic science – fresher than ideas based on existing products**

Technical Innovation Depends on Patents

- **Patents are the most tangible of intangible assets**
- **Patent protection encourages innovation**
- **About 170,000 patents issued by the USPTO in 2002**

There is a Basic Idea for Citation Analysis

- **If I invent a new widget, I must cite all prior art**
- **New patents cite older developments**
- **A patent that receives many forward citations is said to be highly cited**

Sci/Tech Literature Relates Highly Cited Patents to Successful Organizations

- **Highly cited patents correlate with inventor awards, increases in sales, profits, stock rises, patent licensability, and successful products**
- **Citation impact is a proxy for quality, and ultimately value**

Based on articles in Business Week, MIT Technology Review, Bloomberg Personal Finance, and a study commissioned by IEEE and conducted by CHI Research, May 2003

Top Patenting Firms Care About Patents

Top Patenting Firms in 2002

Rank	Company Name	#US Patents	Rank	Company Name	#US Patents
1	IBM	3334	14	Toshiba Corporation	1352
2	Canon Inc	1937	15	Philips Electronics N.V.	1276
3	NEC Corporation	1920	16	Advanced Micro Devices	1152
4	Hitachi Ltd	1882	17	Intel Corp	1088
5	Micron Technology	1851	18	Fuji Photo Film Co Ltd	1010
6	Matsushita Electric	1712	19	Lucent Technologies	818
7	General Electric Co	1681	20	Robert Bosch GmbH	800
8	Sony Corporation	1601	21	Motorola Inc	778
9	Samsung Group	1563	22	Ericsson (LM) Telephone	767
10	Mitsubishi Electric	1474	23	Texas Instruments Inc.	744
11	Hewlett-Packard Co.	1391	24	Eastman Kodak Co	706
12	Fujitsu Limited	1368	25	Honda	703
13	Siemens AG	1357			

Texas Instruments Patent References Several IEEE Articles

United States Patent [19]	[11] Patent Number: 6,101,229
Glover	[45] Date of Patent: Aug. 8, 2000
[54] DATA SYNCHRONIZATION METHOD AND CIRCUIT USING A TIMEOUT COUNTER	H. Kobayashi and D.T. Tang, "Application of Partial-response Channel Coding to Magnetic Recording Systems," <i>IBM J. Res. Develop.</i> , Jul. 1970, pp. 368-375.
[75] Inventor: Kerry C. Glover , Wylie, Tex.	Kenneth Abend and Bruce D. Fritchman, "Statistical Detection for Communication Channels with Intersymbol Interference," <i>Proceedings of the IEEE</i> , vol. 58, No. 5, May 1970, pp. 779-785.
[73] Assignee: Texas Instruments Incorporated , Dallas, Tex.	G. David Forney, Jr., "Maximum-Likelihood Sequence Estimation of Digital Sequences in the Presence of Intersymbol Interference," <i>IEEE Transactions on Information Theory</i> , vol. IT-18, No. 3, May 1972, pp. 363-378.
[21] Appl. No.: 08/819,314	(List continued on next page.)
[22] Filed: Mar. 18, 1997	<i>Primary Examiner</i> —Stephen Chin
Related U.S. Application Data	<i>Assistant Examiner</i> —Mohammad Ghayour
[60] Provisional application No. 60/014,858, Apr. 4, 1996.	<i>Attorney, Agent, or Firm</i> —W. Daniel Swayze, Jr.;
[51] Int. Cl. ⁷ H04L 7/00	[57] ABSTRACT
[52] U.S. Cl. 375/354; 375/365; 375/368; 375/369	A data synchronization method and circuit are provided. A data synchronization circuit (28) includes a header timer (40), a timeout counter (44), a compare circuit (46), and a synchronization field register (48) for use in a read channel (10). During a read operation in the read channel (10), the data synchronization circuit (28) searches for the presence of a synchronization field in a read signal indicating that user data will be provided next. The search occurs over a predefined period of time. The header timer (40) enables a header timer signal for a first predefined period of time. The timeout counter (44) receives the header timer signal and enables a timeout counter signal for a second predefined period of time after the first predefined period of time expires. The compare circuit (46) compares the read signal to the known value or synchronization field stored in the synchronization field register (48). This comparison occurs during the second predefined period of time, the time in which the timeout counter signal is enabled to determine if a synchronization field is present in the read signal. Finally, the compare circuit (46) provides a synchronization detect signal that indicates whether a synchronization field was found during the second period of time.
[56] References Cited	
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5,341,249 8/1994 Abbott et al. 360/46	
5,692,021 11/1997 Walker 375/354	
5,809,091 7/1998 Barrow 375/354	
OTHER PUBLICATIONS	
Lyle L. Frederickson, "Viterbi Detection of Matched Spectral Null codes for PR4 Systems," <i>IEEE Transactions on Magnetics</i> , vol. 28, No. 5, Sep. 1992, pp. 2889-2891.	
K. Chopra and D.D. Woods, "A Maximum Likelihood Peak Detecting Channel," <i>IEEE Transactions on Magnetics</i> , vol. 27, No. 6, Nov. 1991, pp. 4819-4821.	
Arvind M. Patel, "A New Digital Signal Processing Channel for Data Storage Products," <i>IEEE Transactions on Magnetics</i> , vol. 27, No. 6, Nov. 1991, pp. 4579-4584.	
Richard C. Schneider, "Sequence (Viterbi-Equivalent) Decoding," <i>IEEE Transactions on Magnetics</i> , vol. 24, No. 6, Nov. 1988, pp. 2539-2541.	
J.L. Coker, R.L. Galbraith, G.J. Kerwin, J.W. Rae, P.A. Ziperovich, "Implementation of PRML in a Rigid Disk Drive," <i>IEEE Transactions on Magnetics</i> , vol. 27, No. 6, Nov. 1991, pp. 4538-4543.	

Science
Linkage
References
to IEEE
Publications

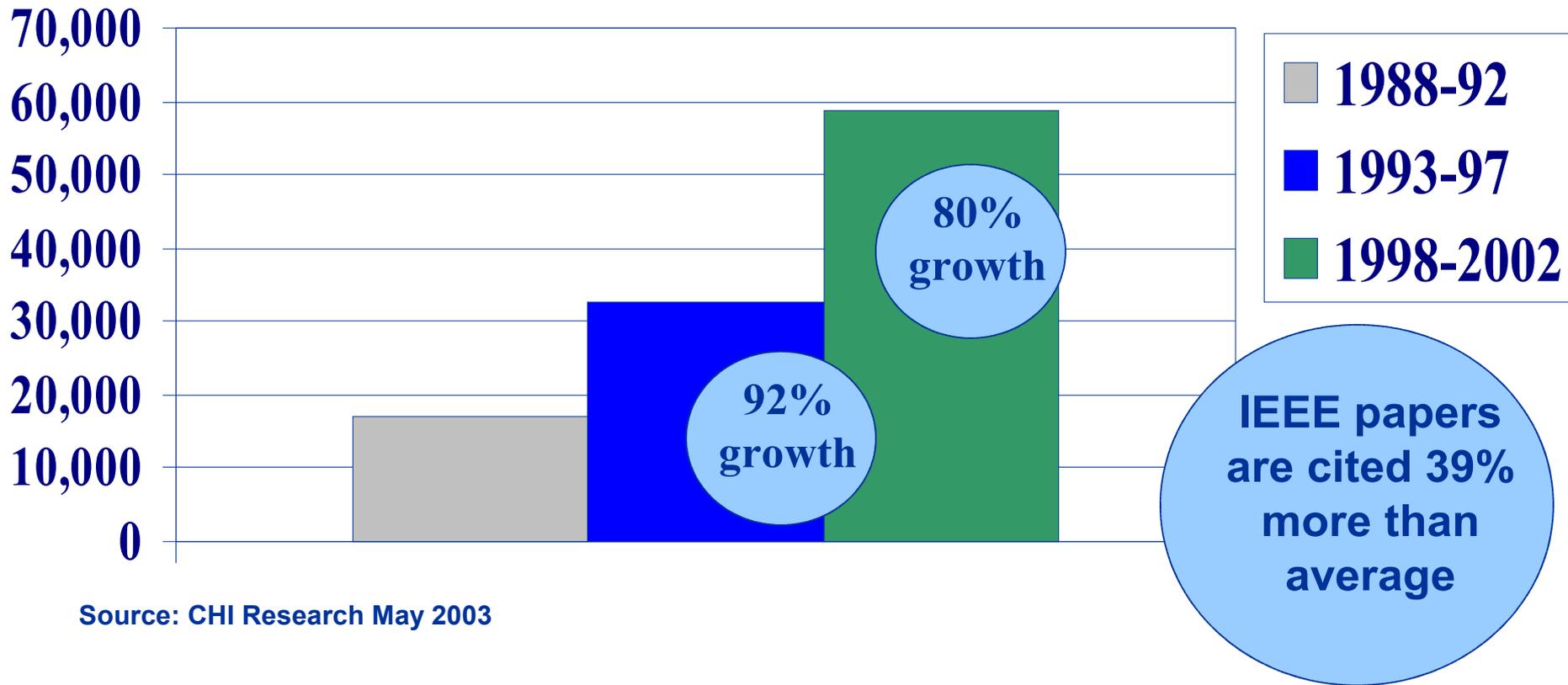
IEEE Drives Blockbuster Patents

- **Over 1,000 USPTO patents are highly cited and reference 3+ IEEE articles.**
- **IEEE provides much of the science base for key technologies**

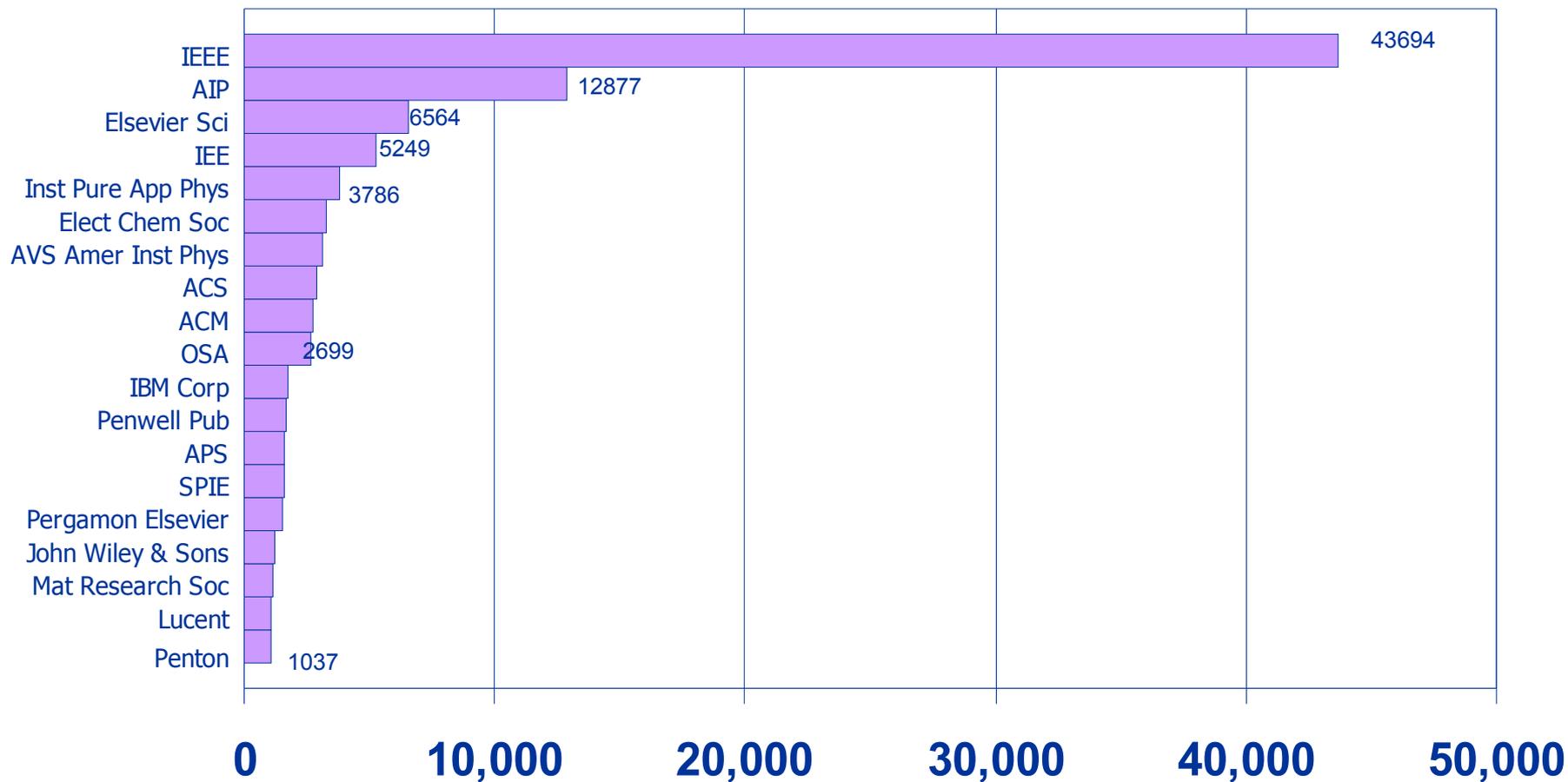
IEEE dominates invention

- **Patenting increased 76% in the last decade**
- **Referencing to IEEE papers increased 267% in the last decade**
- **While patenting is increasingly important, IEEE's importance is growing at a faster rate**

IEEE Patent Citations are Growing at Tremendous Rate



IEEE Tops List of Patent References from Top 25 Organizations



Publishers compiled from all journals referenced 100+ times total from top 25 organizations.

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ISTEC, 19 May 2004

Campinas, Brazil



Patent Citations to IEEE Journals are Broad-Based

62 IEEE Journals with 100+ patent citations

IEEE Journal	Citations from Patents 1985-2002
1. Solid State Circuits	10,639
2. Electron Devices	8,724
3. Proceedings of the IEEE	6,577
4. Communications	6,100
5. Magnetics	5,965
6. Computers	4,602
7. Quantum Electronics	4,040
8. Electron Device Letters	3,803
9. Signal Processing	3,356
10. Photonics Technology Letters	2,927

41% of AMD's Science References are to IEEE Papers

<i>Company</i>	<i>Rank</i>	<i>Journal</i>	<i>#Science Refs</i>	<i>Percent</i>
AMD	1	IEEE J SOLID-STATE CIRCUITS	222	8.6
AMD	2	BYTE	192	7.4
AMD	3	IEEE TRANS ELECTRON DEVICES	192	7.4
AMD	4	IEEE ELECTRON DEV LETT	143	5.5
AMD	5	J ELECTROCHEM SOC	126	4.9
AMD	6	IEEE TRANS COMPUT	117	4.5
AMD	7	IBM J RES DEVELOP	74	2.9
AMD	8	ELECTRONICS DESIGN	71	2.7
AMD	9	APPL PHYS LETT	68	2.6
AMD	10	ELECTRONICS	67	2.6
AMD	11	IEEE MICRO	67	2.6
AMD	12	SOLID STATE TECHNOL	58	2.2
AMD	13	J APPL PHYS	57	2.2
AMD	14	COMPUT DES	44	1.7
AMD	15	IEEE TRANS COMMUN	41	1.6
AMD	16	MAT RES SOC SYMP PROC	41	1.6
AMD	17	IEEE TRANS CIRCUIT SYST	40	1.5
AMD	18	PROC IEEE	39	1.5
AMD	19	COMPUTER ARCHITECTURE NEWS	38	1.5
AMD	20	IEEE TRANS SEMICONDUCT MANUF	37	1.4
		Other IEEE Journals	179	6.9
		Other non-IEEE Journals	678	26.2
		Total	2591	100.0
		Total IEEE	1077	41.6
		Total non-IEEE	1514	58.4

52% of Intel's Patents are Based on IEEE Science

<i>Company</i>	<i>Rank</i>	<i>Journal</i>	<i>#Science Refs</i>	<i>Percent</i>
Intel	1	IEEE MICRO	250	10.6
Intel	2	IEEE J SOLID-STATE CIRCUITS	216	9.2
Intel	3	J ELECTROCHEM SOC	96	4.1
Intel	4	IEEE TRANS COMPUT	76	3.2
Intel	5	IEEE TRANS ELECTRON DEVICES	74	3.1
Intel	6	APPL PHYS LETT	72	3.1
Intel	7	PROC IEEE	65	2.8
Intel	8	IEEE TRANS COMMUN	54	2.3
Intel	9	COMPUTER (IEEE COMPUTER MAG)	51	2.2
Intel	10	ELECTRON LETT	47	2.0
Intel	11	COMMUN ACM	46	2.0
Intel	12	IEEE TRANS CONSUM ELECTRON	45	1.9
Intel	13	IEEE ELECTRON DEV LETT	41	1.7
Intel	14	COMPUT DES	36	1.5
Intel	15	J APPL PHYS	34	1.4
Intel	16	MAT RES SOC SYMP PROC	33	1.4
Intel	17	IEEE SPECTRUM	31	1.3
Intel	18	SOLID STATE TECHNOL	29	1.2
Intel	19	ELECTRONICS DESIGN	27	1.1
Intel	20	IEEE TRANS ACOUST SPEECH SIGN	24	1.0
		Other IEEE Journals	290	12.3
		Other non-IEEE Journals	713	30.3
		Total	2350	100.0
		Total IEEE	1217	51.8
		Total non-IEEE	1133	48.2